REMARKS

Reconsideration of this Application is respectfully requested. In response to the Office Action mailed May 10, 2005, Applicants have amended claims 1, 3, 11, 12, and 13, and cancelled claims 10, 17, and 18 without prejudice to or disclaimer of the subject matter therein. Claims 1-9, 11-16, and 19-24 are pending.

Based on the above Amendment and the following Remarks, Applicants respectfully request that the Examiner reconsider and withdraw all outstanding objections and rejections.

Rejections under 35 U.S.C. § 103

On pages 11-16, the Action rejects claims 2, 4, 5, 10, 11, 17, and 18 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,088,262 to Nasu (hereinafter Nasu) in view of U.S. Patent Application Publication No. 2003/0212897, which is the publication of the instant application. The Action refers to the Publication as "AAP," which will be used in this response for consistency. Applicants note that the Action also appears to reject claim 24 as being obvious over Nasu in view of AAP (see Action, pages 11-13) even though claim 24 is not listed as being rejected in section 11 on page 11 of the Action.

Applicants respectfully traverse the rejection as the Action fails to establish a *prima facie* case of obviousness. In order to establish a *prim facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. See M.P.E.P. § 2143.

Claim 24 recites "A system for obstructing access to a secure area of a semiconductor device comprising: a microprocessor core; a decoder connected to an output of the microprocessor core; a control line connected to an output of the decoder; a circuit for supplying output data; a data output line connected to an output of the circuit for supplying output data; and **an AND gate** having a first input connected to the control line, a second input connected to the data output line, and an output connected to an input of a buffer; and a port implemented in the semiconductor device for

connecting to an in-circuit emulator, wherein a line on the port is also connected to an output of the buffer, wherein when the in-circuit emulator **requests access** to the secure area, **the microprocessor core generates** microprocessor signals for decoding by the decoder, and wherein the decoder decodes the microprocessor signals and generates a control signal on the control line connected to the first input of the AND gate, and wherein the AND gate outputs an obstructing signal to obstruct access by the in-circuit emulator to the secure area." (Emphasis added).

For at least the following two reasons, the Action does not establish a *prima facie* case of obviousness to reject claim 24 based on the combined teachings of Nasu and AAP.

First, neither Nasu nor AAP teach or suggest "**an AND gate** having a first input connected to the control line, a second input connected to the data output line, and **an output** connected to **an input** of **a buffer**," (emphasis added) as recited in claim 24. On page 12, the Action states that column 9, lines 16-22 and FIGs. 10A and 12A of Nasu teach this feature. FIG. 10A of Nasu is titled "Output control circuit & output buffer," but does not disclose even one AND gate. Rather, 301, 302, 303, 304 in FIG. 10A are **NAND** gates, and not AND gates as alleged in the Action. As is known by those skilled in the art, NAND gates include a circle at the output of the logic gate, whereas AND gates do not have the circle. Thus, 301, 302, 303, 304 in FIG. 10A are **NAND** gates.

FIG. 12A of Nasu is titled "Read control circuit." In FIG. 12A, Nasu teaches AND gates (801-803), but does not teach an output of the AND gates being connected to a buffer. Clearly, Nasu does not teach "**an AND gate** having . . . **an output** connected to **an input** of **a buffer**," (emphasis added) as recited in claim 24. Moreover, as understood by one of ordinary skill in the art, replacing the NAND gate in FIG. 10A with an AND gate would not produce the same logical output. The Action does not indicate why one of ordinary skill in the art would be motivated to replace the NAND gate in FIG. 10A with an AND gate. Additionally, the Action does not rely on AAP for a teaching of this feature, and AAP does not teach or suggest an AND gate as claimed. Thus, Nasu and AAP do not teach of suggest "**an AND gate** having a first input connected to the control line, a second input connected to the data output line, and **an output** connected to **an input** of **a buffer**," (emphasis added) as recited in claim 24. Therefore, the Action does not establish a *prima facie* case of obviousness based on the combined teachings of Nasu and AAP to render claim 24 obvious.

Second, neither Nasu nor AAP teach or suggest "wherein when the in-circuit emulator **requests access** to the secure area, **the microprocessor core generates** microprocessor signals for decoding by the decoder," (emphasis added) as recited in claim 24.

As discussed below, AAP only discloses that an in-circuit emulator (ICE) 10 can access a secure area, but does not teach or suggest that a microprocessor 40 generates a signal for decoding by a decoder when ICE 10 requests access to the secure area.

On pages 12-13, the Action equates the claimed in-circuit emulator with the ICE disclosed in paragraph [0007] of AAP, the claimed microprocessor core with element 40 in FIG. 3A of AAP, and the claimed decoder with element 46 in FIG. 3A of AAP for a teaching of the claimed features. However, paragraph [0033] of AAP teaches that:

> "If a user connects an ICE 10 to a semiconductor device 20 for testing or developing code for the semiconductor device 20 and enters a user mode, user mode memory 42 and other general purpose registers may be available to the user at port 22. In addition, should a user issue a command, such as a SWI, to direct the microprocessor core 40 to change into a supervisor mode, the **secure areas** of the semiconductor device 20, for example, supervisor mode memory 44 and secure registers, **may also be available to the user at port 22**, **completely defeating** the purpose of a secure mode." (Emphasis added).

Nowhere does AAP teach that when the ICE 10 **requests access** to a secure area, the microprocessor core 40 **generates** microprocessor signals for decoding by the support logic 46. The ICE 10 of AAP does not request access to a secure area, and the microprocessor 40 of AAP does not generate a microprocessor signal for decoding by the support logic when the ICE 10 requests access to the secure area. AAP only teaches an ICE 10 being able to access the secure areas of the semiconductor device 20 when the microprocessor core 40 changes into a supervisor mode from a user mode (see AAP, paragraph [0033]). Thus, AAP does not teach of suggest "wherein when the in-circuit emulator **requests access** to the secure area, **the microprocessor core generates** microprocessor signals for decoding by the decoder," (emphasis added) as recited in claim 24.

Additionally, Nasu does not teach or suggest "wherein when the in-circuit emulator **requests access** to the secure area, **the microprocessor core generates** microprocessor signals for decoding by the decoder," (emphasis added) as recited in claim 24. As discussed below, Nasu only discloses a read protection control signal being set after a program is written into a memory cell array 100,

and does not teach or suggest a microprocessor generating a signal for a decoder when an in-circuit emulator requests access to a secure area.

On page 13, the Action relies on column 1, lines 55-57 in the summary of the invention of Nasu describing "read protection means" for a teaching of this claimed feature. Column 5, line 4-column 6, line 14 of Nasu describes a read protection control circuit 107, which is the detailed description of the "read protection means" described in the Summary of the Invention. The read protection control circuit 107 of Nasu is responsive to a read protection setting signal 609 (117 in FIG. 1) to determine whether or not a read protection should be set. If the read protection should be set, the read protection control circuit 107 uses a write signal contained in a control signal 606 to store information in EEPROM 601 for read protection (See Nasu, FIGs. 1 and 2). Nasu teaches the read protection is set when the read protection setting signal 609 is H level and the read protection is released when the protection setting signal 609 is L level. In L level, the data written into the EEPROM 601 may be read by the read circuit 602.

A read protection control signal 605 (output 111 from the Read protection control circuit 107 in FIG. 1) becomes H level in the state of read protection and L level in the state of read-out permissible. As the read protection control signal 605 becomes H level any read-out of data from the memory cell array 100 shown in FIG. 1 is inhibited. As the read protection control signal 605 becomes L level, the read-out of data is permitted (or the read protection is released). **After the user of the microcomputer has developed a program and written that program into the memory cell array 100, the read protection is set for the memory cell array 100 by the read protection setting signal 117** (see Nasu, col. 5, lines 64-67). This is to protect the written program from being falsely copied by third parties (see Nasu, col. 5, line 64-col. 6, line 1). Hence, the read protection control circuit 107 of Nasu generates the H level read control protection signal 111 **after** a program is developed and written into memory cell array 100, and **not** when an in-circuit emulator device requests access to the memory cell array 100.

Nowhere does Nasu teach or suggest that the read protection control circuit 107 generates signals for decoding by a decoder when an in-circuit emulator requests access to the memory cell array 100. Hence, Nasu and AAP do not teach or suggest all of the claim features since neither teach or suggest "wherein when the in-circuit emulator **requests access** to the secure area, the

microprocessor core generates microprocessor signals for decoding by the decoder," (emphasis added) as recited in claim 24. Therefore, the Action does not establish a *prima facie* case of obvious for rejecting claim 24 based on the teachings of Nasu in view of AAP.

Accordingly, claim 24 is allowable over the cited references and allowance thereof is respectfully requested.

For reasons discussed below, amended claim 1 is in condition for allowance for reasons analogous to those given for claim 24.

Claims 2, 4, 5, and 11, which depend from claim 1, are also in condition for allowance because of their dependence on an allowable claim.

Claims 10, 17, and 18 have been cancelled and therefore the rejections of these claims are moot.

Rejections under 35 U.S.C. § 102

On pages 6-11, the Action rejects claims 1-4, 6-9, 13-16, and 19-23 under 35 U.S.C. § 102(b) as being anticipated by Nasu.

(A) Claim 1 has been amended to incorporate the features of claim 10. Thus, the claim does not raise any new issues or require any further search.

Amended claim 1 recites: "A method for obstructing access to a secure area of a semiconductor device comprising: connecting an in-circuit emulator to the semiconductor device; generating **a command from the in-circuit emulator** to the semiconductor device, wherein **the command requests access** to the **secure area** of the semiconductor; **providing a control signal** indicating that the semiconductor device has entered a secure mode; and obstructing access to the secure area utilizing the control signal." (Emphasis added).

For reasons analogous to those given for claim 24, claim 1 is in condition for allowance and allowance thereof is respectfully requested.

Claims 2-4 and 6-9, which depend from amended claim 1, are also in condition for allowance because of their dependence on an allowable claim.

(B) Claim 13 has been amended to incorporate the features of claims 17 and 18. Thus, the amendment to the claim does not raise any new issues or require any further search.

Amended claim 13 recites: "A system for obstructing access to a secure area of a semiconductor device comprising: a port for an in-circuit emulator; a first circuit for generating a control signal; and a second circuit for obstructing access to the secure area connected to the control signal, wherein the control signal is utilized by the second circuit to obstruct access to the secure area when a mode indicated by the control signal is a secure mode, and wherein the semiconductor device **enters the secure mode when the in-circuit emulator is connected to the port**." (Emphasis added).

For at least the following reasons, Nasu and AAP, alone or in combination, do not teach or suggest all of the features to anticipate or render obvious amended claim 13.

Nasu and AAP do not teach or suggest "wherein the control signal is utilized by the second circuit to **obstruct access** to the secure area when a mode indicated by the control signal is a secure mode, and wherein the semiconductor device **enters the secure mode when the in-circuit emulator is connected to the port**," (emphasis added) as recited in amended claim 13.

AAP does not teach that the semiconductor device 10 has a control signal utilized by a second circuit to obstruct access to a secure areas when a mode indicated by the control signal is a secure mode. In fact, AAP does not teach or suggest obstructing access to a secure area (see AAP, paragraph 0033). Moreover, the semiconductor device 10 does not enter a secure mode when ICE 10 is connected to port 22. Rather, AAP teaches that if a user connects an ICE 10 to the semiconductor device 20 and enters a user mode, user mode memory 42 and other general purpose registers may be available to the user at port 22 (see AAP, paragraph 0033). AAP also teaches that a user can issue a command to direct the microprocessor core 40 to change into a supervisor mode and that the secure areas are **made available** to the user at port 22 (see AAP, paragraph 0033). Thus, the semiconductor device 20 of AAP does not obstruct access to a secure mode or enter a secure mode when the in-circuit emulator is connected to a port.

Furthermore, Nasu does not teach or suggest "wherein the control signal is utilized by the second circuit to **obstruct access** to the secure area when a mode indicated by the control signal is a secure mode, and wherein the semiconductor device **enters** the secure mode **when** the in-circuit

emulator is connected to the port," (emphasis added) as recited in amended claim 13. Nasu does not teach or suggest that the memory cell array 100 enters a secure mode when an in-circuit emulator is connected to a port. Rather, Nasu teaches that after the user of the microcomputer has developed a program and written that program into the memory cell array 100, the read protection is set for the memory cell array 100 (see Nasu, col. 5, lines 64-67). Hence, the secure mode of Nasu is entered when the program is written into the memory cell array 100, and Nasu does not teach or suggest that the memory cell array 100 **enters** the read protection mode **when** a device is attached to a port. Thus, neither AAP nor Nasu teach or suggest "wherein the control signal is utilized by the second circuit to **obstruct access** to the secure area when a mode indicated by the control signal is a secure mode, and wherein the semiconductor device **enters** the secure mode **when** the in-circuit emulator is connected to the port," (emphasis added) as recited in amended claim 13. Therefore, Nasu and AAP, alone or in combination, do not anticipate or render obvious claim 13.

Accordingly, amended claim 13 is in condition for allowance and allowance thereof is respectfully requested.

Claims 14-16 and 19-23, which depend from amended claim 13, are also in condition for allowance because of their dependence on an allowable claim.

Therefore, claims 1-9, 11-16, and 19-24 are in condition for allowance and allowance thereof is respectfully requested.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is hereby invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment is respectfully requested.

Respectfully submitted,

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